IMEC169.001APC PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| Applicant : | Dierickx et al. |) Group Art Unit Unknown |
|--------------------|--|--------------------------|
| Int'l Appl. No.: | PCT/BE98/00139 |) |
| Int'l Filing Date: | September 22, 1998 |) |
| For : | DEVICES AND METHOD FOR IMPROVING THE IMAGE QUALITY IN AN IMAGE SENSOR |)))) |
| Examiner : | Unknown |) |

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

Please delete Claims 5 and 9.

1. (Amended) An image sensor comprising an array of rows (i) and columns (j) of pixels (X_{ij}) , all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least a first amplifying element (A_j) , all these amplifying elements (A_j) being connected to a common output amplifier (D), characterized in that the sensor further comprises:

a second amplifying element (B_j) on the output of the memory element (M_j) , said common output amplifier (D) having at least two input terminals, means (S1) for switching the pixel's signal on the common output line (l_j) and the memory element's signal (M_i) to respectively third and second amplifying elements $(A_j$ and $B_j)$ of one column, and

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means (S2) for switching the two output signals of the amplifying elements (A_j, B_j) of one column to respectively first and second input terminals of said common [output] amplifier (D).

(Amended) An image sensor comprising an array of rows and columns of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_i) and at least one amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterized in that before the amplifying element (A_j), the common pixel output line (l_j) is divided through switches (S4_j and S5_j) in at least two parallel circuits, at least one circuit having said memory element (M_j), [the two parallel circuits being connected through a switch (S6_j) with the same input of said amplifying element (A_j)].

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: <u>May 12, 1999</u>

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